IC697CPX772

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February 22, 2008
GFK-1430J

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: Series 90™-70 PLC CPU with Firmware Version 8.10

IC697CPX772-JD

This release updates IC697CPX772 hardware. The hardware change, which corrects a rare failure that can occur while communicating on a CPU serial port, does not affect operation or functional compatibility of the CPU.

Firmware Upgrade Kit

To upgrade previous versions of this CPU to firmware version 8.10, you must purchase the field upgrade kit 44A747753-G03 or download it at no charge from the web at http://www.gefanuc.com/

Functional Compatibility

This version of the CPU module is functionally compatible with previous versions.

Product Documentation

The following documentation is available for the IC697CPX772:

Series 90-70 CPU Reference Manual, GFK-0265

Series 90-70 PLC Installation Manual, GFK-0262

Data Sheet, GFK-1429

Operational Notes

Programmer Version Compatibility

Machine Edition Logic Developer – PLC version 2.11 or later, **VersaPro™** version 2.02 or later, **Control** software version 2.40 or later, or **Logicmaster™ 90-70** version 7.02 or later should be used to configure and program IC697CPX772. The following restrictions apply:

- **Machine Edition Logic Developer – PLC** version 2.11 or later, **VersaPro** version 2.02 or later, or **Control** version 2.20 or later is required to support Serial Ports 1 and 2, User Flash Memory, Ethernet Global Data, I/O Scan Sets, VME 3rd Party Interrupts, and Bulk Memory Access.
- **Machine Edition Logic Developer – PLC** version 2.11 or later or **Control** version 2.20 or later is required to support Parameterized Subroutine Blocks (PSBs), Remote Genius I/O Configuration, Stand Alone C Programs, and Multi-threaded LD Programs.
- **Control** version 2.20 or later is required to support Sequential Function Chart (SFC) programming, FIP Configuration, and Clock Synchronization using FIP.
- **Logicmaster 90-70** version 7.02 or later supports Serial Ports 1 and 2 and User Flash Memory, but does not support Ethernet Global Data, I/O Scan Sets, or VME 3rd Party Interrupts.

PCM and BTM Compatibility

With the timing improvements and new features first made available in 90-70 Release 5.00, it is highly recommended that systems using PCMs use IC697PCM711J or later. It is also highly recommended that systems using BTMs use IC697BEM713B or later. Use of boards of an earlier revision may result in lower system performance.

PCM (to CPU) Communications Timeout

The PCM711 with firmware version 4.01 and earlier has a default backplane communications timeout value of 5 seconds. After the PCM has sent a request to the 90-70 CPU, the PCM applies this timeout while it is waiting for a response back from the CPU. In most cases the 90-70 CPU will respond well within the 5-second timeout. However, in certain cases the 90-70 CPU can take longer than 5 seconds to respond. These cases are limited to LOAD/STORE operations of program and/or configuration, especially when blocks in the program are larger than 8K bytes. Folders containing EXE blocks with *.EXE files > 8K bytes are most likely to present problems. Beginning in release 6.00, Standalone C programs larger than 8K bytes also cause this situation.

Beginning in release 5.50 of the 90-70 CPU, the CPU is guaranteed to respond within 8 seconds. Beginning in release 4.03 of the PCM711, the default backplane timeout is 10 seconds. To ensure that PCMs with release 4.01 and earlier firmware do not observe backplane timeouts, a file must be loaded (using *termf*) to the PCM. The file is a binary file and must be named “CPU.ENV.” The contents of the file are (all values specified in hexadecimal):

```
 File                                                                DATA
Offset

0000   4C 5A 01 01 00 00 00 00-00 00 00 00 01 00 00 00    LZ..............
0010   00 00 00 00 00 00 00 00-00 00 43 50 55 4C 49 4E    ..........CPULIN
0020   4B 2E 43 4F 44 00 2D 62-00 36 34 00 2D 74 00 32    K.COD.-b.64.-t.2
0030   30 30 00 00 43 50 55 4C-49 4E 4B 2E 44 43 42 00    00..CPULINK.DCB.
0040   00 4E 55 4C 4C 3A 00 4E-55 4C 4C 3A 00 4E 55 4C    .NULL:.NULL:.NUL
0050   4C 3A 00 00 00 00 00 00-00 00 00 00 00 00 00 00    L:..............
0060   00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00    ................
0070   00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00    ................
```

Once the binary file CPU.ENV (above) is created, use *termf* to load CPU.ENV to the PCM. Then execute a soft reset of the PCM. After executing the soft reset the PCM’s backplane communications timeout should be 10 seconds.

Note: A copy of the above CPU.ENV file can be obtained from the technical support web site.

CAUTION

The CPU.ENV file will not be used when a hard reset is performed on the PCM. With the CPU.ENV file resident in the PCM, a soft reset must be performed after every hard reset of the PCM. Please note that it is possible to issue a “soft reset” COMM_REQ from the Ladder Diagram application; therefore, the application can be modified to handle the required soft reset of PCMs after a power cycle of the PLC system.

Notice to Update GBC Firmware

With the introduction of new features in CPU release 5.00, timings with the Genius Bus Controllers (GBCs) changed; this uncovered a problem in the GBC firmware. GBCs on expanded racks could be lost if the system is fully configured and only the main rack cycles power.

Also, in previous versions of the GBC there was a problem with input data coherency. In a system with a large CPU sweep time and a short Genius bus scan time a problem could be seen if a device is lost. Input data could be defaulted off while the CPU is reading the data from the GBC.

It is recommended that existing GBC hardware be updated to IC697BEM731M or later when updating the PLC CPU firmware to release 8.00 or later. Operation of the IC697BEM731M, in conjunction with release 8.00 or later of the 90-70 CPU, will result in a slight impact to the I/O scan time of the 90-70 PLC.

3rd Party VME Modules

Logicmaster 90 Release 5 (and later) allows 3rd Party VME modules to be configured for six modes: NONE, INTERRUPT ONLY, BUS INTERFACE, FULL MAIL, I/O SCAN, and REDUCED MAIL. However, CPU Release 7.92 does not support REDUCED MAIL.

Maximum PLC Sweep

In systems configured for Genius Bus Redundancy, a complete PLC sweep must be executed every 500 ms or less, even though it is possible to configure the watchdog timer to higher limits. This also means that resetting the watchdog timer with Service Request #8 cannot be done indefinitely.

Serial Comm

The following operational restrictions exist for the Serial Communications feature:

1. Serial communications may add up to 5ms of time to any given sweep. This should be taken into account when setting the watchdog timer.
2. The following procedure is recommended when changing baud rates in the PLC and the WSI board. First enter the configuration package and change the baud rate on the PLC, then store the new configuration. Now power off the PLC and then go to the WSI setup screen and change the WSI baud rate. Finally, power the PLC back on.
3. The link idle time setting in the Hardware Configuration for Serial Communications should be set to 10 seconds or greater. Otherwise, a communications failure will occur when storing the configuration to the PLC.

Serial Port Mode Configuration (Applies to Port 3 Only)

There is a serial port configuration parameter under software configuration for the PLC CPU called MODE. This configuration parameter can be one of two values: **SNP** to indicate that serial port 3 will be used for SNP communications, or **MSG** to indicate that the serial port will be used to send `printf` commands from a C block (or Standalone C Program) to the connected device. If MODE is configured to be **MSG,** and programming software or an HMI/SCADA device is also using port 3 as a means of communicating with the PLC, communications with the PLC will be lost when the PLC goes to RUN mode because serial port 3 is now configured for `printf` commands.

LM90/WSI Attach

Do not connect or disconnect the WSI/BTM cable while the PC/Workmaster host is powered on. This action may cause a running PLC to Stop.

Expansion Rack ID

The expansion racks for the Series 90-70 are shipped with the rack ID strapped for rack 0 (the main rack). If the rack jumper is not changed the PLC will not recognize the rack at all and may not properly identify the error.

Expansion Rack Cable

Connection and disconnection of the expansion rack cable while the CPU is running should not be attempted. This will cause the PLC to go to the STOP/HALT state.

Expansion Rack Power

Expansion racks should be powered up at the same time the main rack is powered up or they should be powered up after the main rack has completed its power up initialization. Do not power up an expansion rack while the PLC CPU is running power-up diagnostics.

Memory Usage

A general rule-of-thumb for memory usage is 48 bytes per I/O point plus register memory in bytes.

Timer Operation

Care should be taken when timers (ONDTR, TMR, and OFDTR) are used in program blocks that are NOT called every sweep. The timers accumulate time across calls to the sub-block unless they are reset. This means that they function like timers operating in a program with a much slower sweep than the timers in the main program block. For program blocks that are inactive for large periods of time, the timers should be programmed in such a manner as to account for this catch up feature.

Related to this are timers that are skipped because of the use of the JUMP instruction. Timers that are skipped will NOT catch up and will therefore not accumulate time in the same manner as if they were executed every sweep.

Fanuc I/O Link

When powering up the PLC CPU without a battery and Fanuc I/O Link boards are present, an incorrect “Loss of Module” fault will be logged for each Fanuc I/O Link board. The PLC CPU will not consider these boards as lost, and the boards will continue to operate properly.

COMM_REQs with Retentive Memory

When powering up the PLC CPU with a program being retrieved from Retentive Memory and proceeding to RUN Mode, any COMM_REQs to a PCM should be delayed for 5 seconds.

Constant Sweep

Constant Sweep time, when used, should be set at least 10 milliseconds greater than the normal sweep time to avoid any over-sweep conditions when monitoring or performing online changes with the programmer. The smallest valid constant sweep time setting is 10 milliseconds. Window completion faults will occur if the constant sweep setting is not high enough.

Interaction of Programming Software with Closed Programming Window

Programming software cannot be used to change the PLC Sweep Modes or timers (Constant Sweep Time, Program Window Times, etc.) while the program window is closed. Use Service Requests #1 - #4 from the PLC application to perform these functions.

CAUTION

Programming software cannot be used to change the PLC mode (STOP, RUN, etc.) while the programming window is closed. Use the toggle switch on the CPU module instead.

Model CPX772/CPX782 CPU Ambient Temperature

Under worse case conditions, at temperatures above 50°C, some limiting of system power may be necessary. Please see the data sheet for this product for more information.

SFC RESET Function Block

The SFC RESET function block only executes when used in Action Logic or Pre/Post Logic within an SFC block (Main SFC or SFC sub-block). Attempting to execute an SFC RESET function block from a Ladder Diagram Main/sub-block will not reset the SFC network and (as of v6.02) will not pass power flow to any logic right of the SFC RESET.

Ethernet Global Data and Sweep Time

Each Ethernet Global Data exchange configured for either consumption or production can add up to 1msec to the sweep time. This sweep impact should be taken into account when configuring the PLC for constant sweep mode and setting the CPU watchdog timeout.

CMM and PCM Module Compatibility

Due to the increased reference table sizes on the CPX CPU models, older versions of CMM and PCM modules may experience compatibility problems with the CPX model CPUs. Firmware upgrades are available for customers with other versions of these modules.

CMM modules (IC697CMM711) of revision **'F'** or later will not experience this problem.

PCM modules (IC697PCM711) of revision **'P'** or later will not experience this problem.

Serial Ports 1 and 2

This CPU is equipped with two additional serial ports (ports 1 and 2) as well as the standard serial port (port 3) found on previous Series 90-70 models. Port 1 supports the RS-232 standard, and port 2 supports the RS-485 standard. These additional serial ports support the following baud rates: 1200, 2400, 9600, 19200, 38400, and 57600. Note that they do not yet support 115k baud. Both ports can e operated simultaneously without dropping characters up to 57600 baud.

SNP Slave protocol support for these ports was added in firmware release 7.80. Break-free SNP (slave) was added as the default protocol to ports 1 and 2 in firmware release 8.00 (port 3 does not support break-free SNP). All functionality of serial port 3 is available through ports 1 and 2 with these exceptions: (1) they do not support connection of the C debugger; (2) they do not support `printf` functionality for C programming.

All three serial ports can be configured by programming software to select baud rate, parity, stop bits, etc.

If upgrading this module from a previous version that did not support these two ports, you may have to set the ports' configuration parameters (using a programmer connected to port 3) before you will be able to use the ports.

Programmer Communications Issues (Serial Ports 1 and 2)

When using serial ports 1 or 2 for programmer communications, a momentary loss of communications may be observed after a store of hardware configuration while configuration settings are being updated. This is normal operation. Port configuration changes for ports 1 and 2 are processed after the store of hardware configuration. Changes to the configuration of port 3 are processed on a reconnection of port 3.

Note that all port communications settings should be carefully verified before performing a hardware configuration store. If any of the essential configuration settings (such as mode, baud rate, parity, etc) for the port connected to the programmer are changed, you will lose communications after a configuration store. Communications will be restored once the host (programmer) settings are changed to match the port's new settings.

Word-wide reads from a 3rd Party VME Module

An attempt to read a word value from a 3rd party VME module that does not support word-wide accesses will cause the module to generate a System Bus Error fault if it responds to a GE Fanuc slot-based address. This has the following implications:

1. The 90-70 CPU always interrogates the first several bytes of every GE Fanuc slot assignment using word accesses during system configuration. Accordingly, users may observe a System Bus Error fault from such a module immediately after power up.
2. If a System Bus Error fault occurs immediately after power up in a PLC that uses a 3rd party module, the user should determine whether that module does not support word-wide accesses, responds to a GE Fanuc slot-based address, and asserts bus errors. If the module has all these characteristics, then the bus error fault should be ignored. Designers of applications that use such modules should advise their users to ignore this fault.
3. To avoid this System Bus Error fault, designers of applications using 3rd party VME modules that do not support word-wide accesses should do one of the following:

(a) Configure the module so that it does not respond at all to word-wide access from the CPU. There are two ways to do this: 1) Configure the VME base address of the module in the range 100000 - 7FFFFF (hex) so that it is not at the beginning of any GE Fanuc slot-based address space; or 2) Configure the module to use Address Modifier code 3Dh rather than 39h or 29h. These are the preferred solutions and are often the easiest.

(b) Configure the VME module so that it does not assert BUSER. One possible way to do this is to disconnect the VME BUSER line from the module (which will force it high). However, this will not work if the module also asserts DTACK for these word-wide cycles.

Cannot write to 90-70 CPX flash memory when EGD is configured

The Series 90-70 CPX models do not support write to user flash when EGD is configured for a CMM742. Attempting the write operation will produce the following error:

```
Error 8544: Flash operation failed [ Server Error: Flash memory is incompatible ]
```

To use flash memory, the entire EGD configuration must be removed, including the adapter name in the IC697CMM742 properties. As an alternative to EGD, consider using SRTP for Ethernet data communication when user flash memory is required.

New Features and Functionality of Firmware Release 8.10

Increased Maximum %R Size

Increased the maximum size of the register table from 16384 to 32640. This feature requires version 2.2 or later of IC641CTL software or version 2.0 or later of IC641VPH/VPP software.

TOD Clock Changed

The default time-of-day (TOD) clock has been updated to January 1, 2000

Service Request 7 Given POSIX Capability

Service Request 7 supports reading or writing the Real Time Clock in POSIX format. This feature has been available since 7.90, but was previously undocumented. To use this request, the following data block must be included:

Data	*Memory Location*
0 = Read time and date 1 = Set time and date	Address*
4 = POSIX format (see manual for other formats)	Address + 1
Number of seconds (signed double word value).	Address + 2
Number of nanoseconds (signed double word value	) Address + 4

* Address refers to the first word of the data block. For example, if Address were %R00100, Address + 1 would be %R00101, Address + 2 would be %R00102, and Address + 4 would be %R00104.

Problems Resolved by Firmware Release 8.10

Incorrect Checksums from Service Request 23

Service Request 23, which returns checksums, does not include the checksums from all of the configuration units and sometimes returns the incorrect value for the program checksum.

COMM_REQs Located in Interrupt Blocks

If the target of a COMM_REQ used in an interrupt block is a smart option module, the COMM_REQ may fail and cause a CPU software fault.

PSB Power Flow Output

The Power Flow out parameter from a Parameterized Subroutine Block (PSB) may be overwritten by a call to another PSB if the parameter is set prior to the call of the subsequent PSB.

PSB Y0 Not Saved and Restored Across Calls to Nested PSBs

PSB Y0 is not saved and restored across calls to nested PSBs (Parameterized Subroutine Blocks). A single location in bit cache memory is used for storing the Y0 value, and this bit is set to “1” upon each invocation of a PSB block. Use a different variable to store the value of Y0 across the call and set Y0 immediately prior to exiting the block. Care should be taken when using Y0 both within a PSB block called by an interrupt block and in the block called by the main LD program.

Restrictions and Open Problems

1. When a C block containing floating-point math operations executes in Microcycle mode, and the microcycle base scan is shorter than the PLC sweep time, the C floating-point math functions may detect false errors and log PLC faults. These errors disappear when the microcycle base scan is longer than the PLC sweep time.
2. If an expansion rack powers up while the CPU in the main rack is in the RUN mode, the slot fault contacts will prematurely indicate that the modules in the expansion rack are not faulted before they complete their power up.
3. When there is no logic stored in a CPU module the %Q and %M tables will be cleared when the CPU is placed in RUN mode. In this context, "no logic stored" means that no program had ever been stored or that the clear function on Logicmaster 90 had been used to clear logic and configuration.
4. When the Bit Sequencer sequences from one step to another, the negative transitional contact that corresponds to the original step is not set. The transition contact for the new step is set and remains set until the sequencer sequences to the next step. This operation is identical to the operation of the previous versions of the CPU firmware.
5. If multiple faults exist in a 90-70 Remote Drop and one of them is corrected, a FAULT contact that uses the Remote Drop's module reference will incorrectly indicate that no faults exist at the Remote Drop.
6. An incorrectly formatted COMMREQ (e.g. incorrect task id field) directed to a PCM or CMM module does not result in an error being logged in the PLC fault table. Correctly formatted COMM_REQs operate normally.
7. The bit sequencer function block clears bits outside the range of the functions length parameter when the reset condition is TRUE. The affected bits lie within the bytes accessed by the function. For example, with length 100 (bits), the four bits at 101, 102, 103, and 104 are cleared by the bitseq function when it is reset. This operation is identical to the operation of the previous versions of the CPU firmware.
8. A large number of COMM_REQs (typically greater than 8) sent to a given board in the same sweep may cause Module Software fault to be logged in the PLC fault table. The fault group is MOD_OTHR_SOFTWR (16t, 10h) and the error code is COMMREQ_MB_FULL_START (2). When this occurs, the "FT" output of the function block will also be set. To prevent this situation, COMM_REQs issued to a given board should be spread across multiple sweeps so that only a limited number (typically 8 or less) of COMM_REQs are sent to a given board in each sweep. In addition, the FT output parameter should be checked for errors. If the FT output is set (meaning an error has been detected), the COMM_REQ could be re-issued by the application logic.
9. When attempting simultaneous loads of logic through multiple Ethernet connections and a serial connection, the loads through the Ethernet connection may fail with a communication timeout.
10. On occasion, the PLC may fail to respond to an SNP Attach message issued through the additional Serial Ports (Port 1 or Port 2). Several retries of the SNP Attach message may be necessary to successfully attach to the PLC via these two ports. Therefore, a user developing their own SNP applications to run on these two ports should design and code for multiple SNP Attach retries.
11. An attempt to read a word value from a 3rd party VME module which does not support word wide accesses occurs, and the module responds to a GE Fanuc slot assigned address, the module will generate a System Bus Error fault. Please see "Operational Notes" on page 1 for more information on this issue.